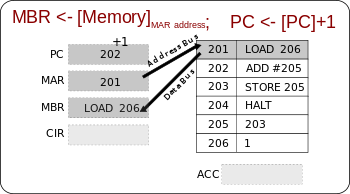
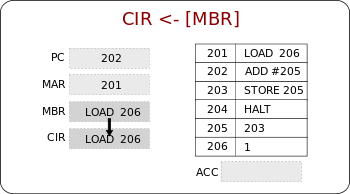
Task 3 Brief - Fetch Decode Execute Cycle

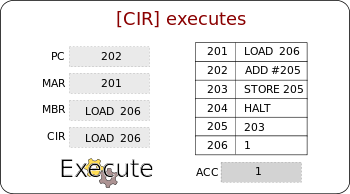
The initial contents of the Program Counter (201), which is the address of the next instruction to be executed, is placed into the Memory Address Register. In the meantime, the Program Counter is increased by 1 to 202.

[](http://commons.wikimedia.org/wiki/File:CPT-fetch-execute-MBR-Memory.svg)

The address is sent from the MAR along the address bus to the Main Memory. The instruction at that address is found and returned along the data bus to the Memory Buffer Register.

[](http://commons.wikimedia.org/wiki/File:CPT-fetch-execute-CIR-MBR.svg)

The MBR loads the Current Instruction Register with the instruction to be executed.

[](http://commons.wikimedia.org/wiki/File:CPT-fetch-execute-CIR-executes.svg)

The instruction is decoded and executed using the ALU if necessary.

The Cycle starts again!

Assignment Task 3 – Complete the diagram

Task 3.1 – Explain the Fetch Decode Execute Cycle using the register names and memory as steps.

|  |  |
| --- | --- |
|  |  |
|  |  |
|  |  |
|  |  |

Task 3.2 – Complete the information in the registers below for three CPU cycles, based on the data in the RAM locations 67-72. It is better to provide separate diagrams from the one below, because some of the data in the RAM locations will change.

|  |  |
| --- | --- |
| 67 | LOAD 71 |
| 68 | ADD 72 |
| 69 | STORE 72 |
| 70 | HALT |
| 71 | 92 |
| 72 | 5 |

67

PC

MAR

MBR

CIR

ACC

Task 3.3 – Complete the part of the technical report for the above tasks.